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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,241	10/17/2001	Robbert Christiaan Van Ommering	PHNL 000550	7627

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS

P.O. BOX 3001

BRIARCLIFF MANOR, NY 10510

EXAMINER

BULLOCK JR, LEWIS ALEXANDER

ART UNIT	PAPER NUMBER
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2195

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,241	VAN OMMERING, ROBBERT CHRISTIAAN	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on response filed 12/2/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 9 is/are rejected.
- 7) ☒ Claim(s) 2,8,10 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. **In particular foreign application EP 0271945 B1 has not been considered and must be submitted for consideration.**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(b) as being anticipated by WOLD (U.S. Patent 5,386,568).

As to claim 1, WOLD teaches in an audio apparatus (music synthesizer) (col. 19, lines 57-61; col. 5, lines 26-31), a method of controlling an arrangement of a plurality of hardware components (hardware devices / hardware components) at least some of which are coupled to one another via signal leads (cables / wires), by means of a data processing unit (embedded processors) (col. 19, lines 28-31; col. 19, lines 42-46; col. 19, line 55 – col. 20, line 3) and a computer program (software) which is executed

Art Unit: 2195

therein, characterized in that the computer program comprises sub-modules (software modules) (col. 11, lines 2-5; col. 4, lines 65-67) which correspond (are associated) to the hardware components (hardware devices / hardware components) and are connected via data channels (via input / output communication software connections) in conformity with the real signal leads (cables / wires) between the hardware components (hardware devices) (col. 11, lines 7-33; col. 12, lines 43-66; col. 19, lines 2-5; col. 19, lines 34-42; col. 9, lines 61-68; col. 20, lines 14-17; col. 19, lines 52-68; col. 24, lines 42-55).

As to claim 3, WOLD teaches all data channels utilize the same communication protocol (col. 20, lines 17-19; col. 11, lines 2-25).

As to claim 4, WOLD teaches that the hardware components are printed circuit boards, layout cells, microchips and/or core cells (col. 19, lines 57-61).

As to claims 5 and 6, reference is made to an audio apparatus that corresponds to the method of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 7, WOLD teaches the sub-modules (software modules) have inputs and outputs (input / output objects) that correspond to input and outputs (input / output ports) for the hardware components (hardware modules) (col. 19, lines 61-64; col. 24, lines 42-52; col. 19, lines 28-46).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over WOLD (U.S. patent 5,386,568) in view of Official Notice.

As to claim 9, WOLD teaches hardware devices can establish connection through inputs and outputs (input object / output object / input port / output port) to the sub-modules (software modules) and the hardware components (hardware modules) (col. 19, lines 61-64; col. 24, lines 42-52; col. 19, lines 28-46). WOLD also states that the invention is not to be limited to a specific illustrated embodiment, but only to the scope of the claims. However, WOLD does not teach that the hardware devices are switches. Official Notice is taken in that switches are well-known hardware devices and therefore would be obvious in view of the teachings of WOLD in order to facilitate the communication between switches by using software modules and hardware components.

Allowable Subject Matter

5. Claims 2, 8, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Claim 2 details that the data channels between the sub-modules are adapted in conformity with the dynamic changing of the hardware components and/or the signal leads between the hardware components. The cited prior art of record does not teach the cited limitations. The prior art of record at best teaches linking devices based on the linking of software modules or the dynamic changing of lower level modules facilitate the changing of higher level modules and vice versa. The cited prior art does not allude to the dynamic changing of leads affecting the channels of sub-modules. Claims 8, 10 and 11, detail a signals validity / properties are reported / defined through the inputs and outputs to the sub-modules and the hardware components. None of the cited prior art of record teaches this cited functionality. The prior art of record at best teaches linking devices based on the linking of software modules or the dynamic changing of lower level modules facilitate the changing of higher level modules and vice versa. It makes no reference to reporting or defining a signals validity or property.

Response to Arguments

7. Applicant's arguments filed 12/2/04 have been fully considered but they are not persuasive. Applicant argues that Wold does not teach or suggest sub-modules that

correspond to the hardware components but state that interconnections can be made with software modules. The examiner disagrees. Column 19, lines 52-68, teaches that a plurality of independent hardware modules having ports, which correspond to an input object or an output object. That is, each port has a hardware interface for sending or receiving signals to external devices, and internally is controlled by a software module that interfaces to the port through one or more Input objects or Output objects. Column 24, lines 42-55, clearly sets forth that the communication of data between software modules is through hardware devices corresponding to the software modules wherein each has at least one input port corresponding to at least one Input object and at least one output port corresponding to at least one output object wherein the ports have a communication linkage. Therefore, the cited reference teaches sub-modules that correspond to the hardware components and the connections of the sub-modules and hardware components as disclosed in the cited claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

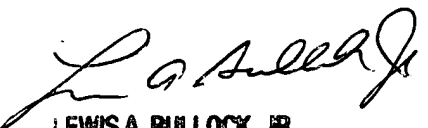
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 31, 2005


LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER